US-PAT-NO: 6788752
DOCUMENT-IDENTIFIER: US 6788752 B1
TITLE: Multi-carrier transmission system

Detailed Description Text - DETX (4):

The transmitter 1 incorporates several components including an encoder (not shown), a discrete multi-tone modulator 10, a cyclic prefix adder 11 a parallel to serial converter 12, a digital to analogue converter 13 and an analogue transmitter with high-pass filter 14. The encoder is connected upstream of the discrete multi-tone modulator 10 and serves to translate incoming bit streams into in phase, in quadrature sequences for each of a plurality of sub-channels. These encoded sequences are input to the multi-tone modulator 10, which is preferably an IFFT modulator 10 that computes the inverse fast Fourier transform by an appropriate algorithm. The discrete multi-tone encoded symbols generated in the IFFT modulator 10 are then each cyclically extended by the addition of a cyclic prefix in CP circuitry 11. This is done by duplicating a number of samples at the end of a symbol and adding these to the beginning of the symbol. The number of bits included in the cyclic prefix depends on the application and acceptable bandwidth penalty. Typically a cyclic prefix does not exceed 10% of a symbol. The parallel symbol sequences are then converted to a serial bit stream in a parallel to serial converter 12. The serial bit stream is then converted to an analogue signal with digital to analogue converter 13, prior to transmission over the link by an analogue transmitter 14, which incorporates a high-pass filter for filtering out signals in the transmitter 1 that can interfere with the POTS band. The signal is then sent over a channel 30 having a transfer function 'h' to a remote location. At the receiver 2 positioned at the remote location, an analogue receiver 20, which also incorporates a high-pass filter for filtering out noise from the POTS band, receives the signal and inputs this into an [illegible] converter 21 for digital conversion. The digital bit stream is then sent to the ISI compensation block consisting of delay circuitry 22, a time domain [illegible] (TEQ) 23, which may be a finite impulse response ([illegible] tail [illegible] circuitry 24 and an adder 25. This block will be described in more detail below, however it should be noted that the time domain [illegible] 23 is optional in this arrangement. It is useful for equalizing the received signal but is not necessary for reducing the ISI. The received symbols are then returned to parallel format in a serial to parallel converter 26. The cyclic prefix is discarded in CP removal circuitry 27 and the symbols are then demodulated in FFT circuitry 28 which performs a fast Fourier transform, and decoded by a decoder (not shown).

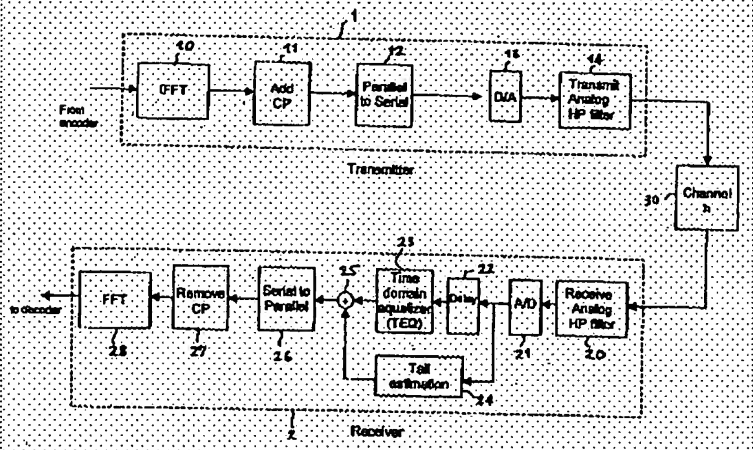

Fig. 1